AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0030] with the following amended paragraph:

[0030] Fig 1 shows programming circuitry in a MBPC Flash memory 100 including a memory array 110 with continuous word lines 114 connected to row decoders and drivers 160. Memory array 110 includes memory cells 112 that can be conventional floating gate transistors or any non-volatile memory cell capable of representing data as a programmable threshold voltage. Memory cells 112 in array 110 are arranged in rows and columns. Each row of memory array 110 contains memory cells 112 with gates connected to the word line 114 corresponding to the row. Word lines 114 are generally fabricated as polysilicon or silicide lines with portions of the word lines 114 forming the control gates of floating gate transistors that are memory cells 112. Each column of memory array 110 contains memory cells having drains connected to a column line (or bit line) 116 corresponding to the column. Column lines 116 can include diffused lines or metal lines with contacts to diffused drain regions depending on the architecture of memory array 110 (e.g., whether a contactless architecture or not).

Please replace paragraph [0039] with the following amended paragraph:

[0039] With the high gate voltage Vpp, current through the selected memory cells causes channel hot electron (CHE) injection into the floating gates of the selected memory cells, which increases the threshold voltages of the selected memory cells. Fig. 4 illustrates typical plots 407, 408, 409, and 410 of the threshold voltage Vt versus accumulated programming time for a Flash memory cell with respective applied gate voltage Vg of 7, 8, 9, and 10 volts, ~~respectively~~ at an applied drain voltage Vd of 4.5V and a source voltage Vs of 0V. Plots 407 to 410 illustrate that higher word line voltages cause faster changes in the threshold voltage Vt and allow

programming of the memory cell to higher threshold voltages. For all gate voltages, the change in threshold voltage Vt per time is fasted when the threshold voltage of the memory cell is the lowest. The rate of increase typically saturates after a sufficiently long accumulated programming time (e.g., after about 1 μs). In this saturation region, changes in threshold voltage Vt have an intrinsic one-to-one correspondence to changes in Vg. This phenomenon can be used to achieve a small change (ΔVt) in threshold voltage per programming cycle 310 or accurate programming of target threshold voltages.

Please replace paragraph [0040] with the following amended paragraph:

[0040] During verify cycles 320 of Fig. 3A, sensing operations determine whether the selected memory cells have reached their respective target threshold voltages. The length of each verify cycle 320 generally depends on the type of sensing operation used to sense threshold voltage states of the selected memory cells. The sensing operation used in Fig. 3A applies to a read voltage ~~Vr~~ V_R (typically about 5 to 7 volts) to the word line connected memory cells selected for programming. A read voltage Vbias (typically about 1 to 1.5 volts) is applied to the column lines of the selected memory cells, and the source lines of the selected memory cells are at the virtual ground voltage near reference voltage Vss. A sense amplifier, which can also be used for read operations, then compares a voltage or current on a selected column line to a reference voltage or current corresponding to the N-bit data value being written in the selected memory cell.

Please replace paragraph [0090] with the following amended paragraph:

[0090] The principles of the two types of write operation described above can be combined so that a write operation using multi-bit-data-dependent bit and/or source line biasing still reaches different threshold voltages at different times. Fig. 9A shows

a timing diagram for a 4-bit (or 16 levels) per cell memory having a total available write time of Ttot divided into four intervals I0, I1, I2, I3. The shared world line signal is asserted to voltage Vpp0, Vpp1, Vpp2, and Vpp3 for programming cycles 910-0, 910-1, 910-2, and 910-3 during intervals I0, I1, I2, and I3, respectively. The selected word line has a read voltage ~~Vr~~ V_R for verify cycles 920.

Please replace paragraph [0100] with the following amended paragraph:

[0100] Write operation portion 1050 in Fig. 10A uses a word line signal WLS having a staircase-increasing word line programming voltage that is applied during a series of programming cycles 1010 having uniform duration as in the write operation of Fig. 8B. Other types of write operations such as the write operations of Fig. 3A to 3G, 6, and 8A to 8E could similarly use remedial programming cycles, which are added at the ends of the write operations to avoid errors resulting from slow programming memory cells. Further, remedial programming ~~1040~~ 1060 can be applied at the end of any or all of the intervals at which memory cells are expected to reach particular target threshold voltages. Remedial programming sequences could, for example, be added at the ends of intervals, I0, I1, I2, and I3 of the write operations such as the write operations illustrated in Figs. 5A, 5B, 5C, 9A, and 9B.

Please replace paragraph [0102] with the following amended paragraph:

[0102] Column line bias voltages Vw1, Vw2, and Vw3 and the source line bias voltages ~~VSL0,~~ VSL1, VSL2, and VSL3 are selected and used in combinations such that typical memory cells are programmed to respective target threshold voltages Vt1 to Vt15 before the end of write operation portion 1050.

Please replace paragraph [0116] with the following amended paragraph:

[0116] Programming circuitry 1400 includes a variable bit line load 1420 and a variable source line bias circuit 1450. Variable bit line load 1420 is connected to multi-level verify/read circuits 1440. Signals PGM, Source Bias Disable, VFY+Read and VFY+Read+Source Bias Disable control variable source line bias circuit 1450. A full 4-BPC memory would further include at least X similar variable bit line load and source line bias circuits, where X is the number of memory cells simultaneously accessed during a write operation. For memory cell 1410, I/O lines 1435 and a column select device 1430, which is under control of a signal Column Select N, connect variable bit line load 1420 to bit line 1416 when a write operation selects memory cell 1410. The source line 1418 of memory cell 1410 is connected to source line bias circuit 1450.